

CLAIMS

What is claimed is:

- 1 1. A process for reducing cross-talk noise in a circuit, comprising:
2 identifying a victim net in an integrated circuit;
3 determining a change in ground capacitance for the victim net to identify a noise
4 amplitude less than or equal to a maximum allowable noise height;
5 selecting from a library at least one cell having an input capacitance for the victim net
6 closest to the change in ground capacitance; and
7 coupling the at least one cell with the victim net.
- 1 2. The process of claim 1, wherein the at least one cell couples with the victim net using
2 incremental routing.
- 1 3. The process of claim 1, wherein a value for the noise amplitude is determined through
2 a calculation comprising:
3 $(R_d C_c) / (R_d (C_g + C_c) + (\text{Slew}_{\text{agg}}/2))$,
4 wherein R_d comprises a holding resistance of a driver of the victim net, C_c comprises
5 a coupling capacitance between the victim net and an aggressor net, C_g
6 comprises a ground capacitance of the victim net, and Slew_{agg} comprises a
7 slew of the aggressor net.

1 4. The process of claim 1, wherein determining the change in ground capacitance further
2 a calculation comprising:

3
$$(-C_c * N_s) / (N_m * N_A),$$

4 wherein, C_c comprises a coupling capacitance, N_s comprises a noise slack, N_m
5 comprises a noise margin, and N_A comprises the noise amplitude.

1 5. The process of claim 4, wherein the noise slack comprises a difference between noise
2 margin and noise amplitude.

1 6. The process of claim 1, further comprising testing an integrated circuit in response to
2 connecting the at least one cell with the victim net.

1 7. The process of claim 6, wherein testing the integrated circuit further comprises one
2 from a group consisting of conducting a timing analysis, conducting a change in slew
3 analysis, conducting a power consumption analysis, and conducting an
4 electromigration analysis.

1 8. The process of claim 6, further comprising rejecting the coupling of the at least one
2 cell with the victim net in response to a result of the testing providing a value
3 corresponding to an adverse effect on the integrated circuit.

1 9. A system for reducing cross-talk noise in a circuit, comprising:
2 a noise analyzer configured to identify a victim net in an integrated circuit;
3 an analysis engine configured to determine a value for a change in ground
4 capacitance for a victim net, the change in ground capacitance providing a

5 noise amplitude for the victim net less than or equal to a maximum allowed
6 noise height; and

7 a library configured to provide at least one cell having an input capacitance for
8 coupling with the victim net, a total input capacitance for the victim net
9 having a value substantially close to the change in ground capacitance.

1 10. The system of claim 9, wherein the noise analyzer is further configured to determine
2 the value of the change in ground capacitance through a calculation comprising:

3
$$(-C_c * N_s) / (N_m * N_A),$$

4 wherein, C_c comprises a coupling capacitance, N_s comprises a noise slack, N_m
5 comprises a noise margin, and N_A comprises the noise amplitude.

1 11. The process of claim 10, wherein the noise slack comprises a difference between
2 noise margin and noise amplitude

1 12. The system of claim 9, wherein a value for the noise amplitude is determined through
2 a calculation comprising:

3
$$(R_d C_c) / (R_d (C_g + C_c) + (Slew_{agg}/2)),$$

4 wherein R_d comprises a holding resistance of a driver of the victim net, C_c comprises
5 a coupling capacitance between the victim net and an aggressor net, C_g
6 comprises a ground capacitance of the victim net, and $Slew_{agg}$ comprises a
7 slew of the aggressor net.

- 1 13. The system of claim 9, further comprising a connection module configured to couple
2 the at least one cell to the victim net.
- 1 14. The system of claim 13, further comprising a test module configured to test an
2 integrated circuit incorporating the victim net in response to the coupling of the at
3 least one cell to the victim net.
- 1 15. The system of claim 14, wherein the test comprises at least one test of a group
2 consisting of a timing test, a slew test, power consumption test, and an
3 electromigration test.
- 1 16. The system of claim 14, wherein the test module is further configured to reject
2 coupling of the cell to the victim net in response to a result of the test providing a
3 value corresponding to an adverse effect on the integrated circuit.
- 1 17. A system for reducing cross-talk noise in a very large scale integration ("VLSI")
2 circuit, the system comprising:
3 a means for performing a noise analysis on a plurality of nets in the VLSI circuit;
4 a means for identifying at least one victim net among the plurality of nets, the victim
5 net having a noise amplitude greater than a maximum allowable noise height;
6 a means for selecting a victim net from the at least one victim net;
7 a means for determining a change in a ground capacitance for the victim net such that
8 the noise amplitude of the victim net is less than the maximum allowable
9 noise height;

10 a means for selecting from a cell library a cell providing an input capacitance value
11 substantially close to the value of the change in the ground capacitance; and
12 a means for coupling the cell with the victim net.

1 18. The system of claim 17, further comprising a means for testing the VLSI circuit in
2 response to coupling the cell with the victim net.

1 19. The system of claim 18, wherein the means for testing the VLSI circuit rejects
2 coupling the cell with the victim net in response to a test value associated with an
3 adverse affect on the VLSI circuit.

1 20. The system of claim 19, wherein the means for testing the VLSI circuit includes a
2 process for conducting a circuit timing test and the test value associated with the
3 adverse affect on the VLSI circuit comprises a value less than a predetermined timing
4 value.

1 21. The system of claim 19, wherein the means for testing the VLSI circuit includes a
2 process for conducting a power consumption test and the test value associated with
3 the adverse affect on the VLSI circuit comprises a value less than a predetermined
4 power consumption value.

1 22. The system of claim 17, wherein the cell comprises one from a group consisting of an
2 inverter logic element and a capacitance cell.

1 23. A process for reducing cross-talk noise in a very large scale integration ("VLSI")
2 circuit, the process comprising:

3 performing a noise analysis on a plurality of nets in the VLSI circuit;
4 identifying at least one victim net among the plurality of nets, the victim net having a
5 noise amplitude greater than a maximum allowable noise height;
6 selecting a victim net from the at least one victim net;
7 determining a change in a ground capacitance for the victim net such that the noise
8 amplitude of the victim net is less than the maximum allowable noise height;
9 selecting from a cell library a cell providing an input capacitance value substantially
10 close to the value of the change in the ground capacitance; and
11 coupling the cell with the victim net.

1 24. The process of claim 23, further comprising testing the VLSI circuit in response to
2 the coupling of the cell with the victim net.

1 25. The process of claim 24, wherein the step of testing the VLSI circuit further
2 comprises rejecting the coupling of the cell with the victim net in response to a test
3 value associated with an adverse affect on the VLSI circuit.

1 26. The process of claim 25, wherein the step of testing the VLSI circuit comprises
2 performing a timing test and the test value associated with the adverse affect on the
3 VLSI circuit comprises a value less than a predetermined timing value.

1 27. The process of claim 25, wherein the step of testing the VLSI circuit comprises
2 performing a power consumption test and the test value associated with the adverse

3 affect on the VLSI circuit comprises a value less than a predetermined power
4 consumption value.

1 28. The system of claim 23, wherein the cell comprises one from a group consisting of an
2 inverter logic element and a capacitance cell.